

BI
con-1

of the device in units of pixels and also destination image data is stored in a second storage unit of the image processing device in units of pixels, and a generation step for generating rendering commands that cause the action of applying a stipulated pixel-unit operation to the source image data stored in the first storage unit in the storage step and rendering the data as destination image data in the second storage unit in units of polygons to be performed repeatedly until a stipulated arithmetic result is obtained.

Please replace the paragraph beginning at page 13, line 1 with the following:

BO

Rendering engine 41 of image processing chip 33 executes operations for rendering stipulated image data in image memory 43 via memory interface 42 according to rendering commands supplied from main CPU 31. Bus 45 is connected between memory interface 42 and rendering engine 41, and bus 46 is connected between memory interface 42 and image memory 43. Bus 46 has a bit width of 128 bits, for example, so that rendering can be executed at high speed in image memory 43. Rendering engine 41 has the capability to render 320×240 pixel or 640×480 pixel image data in NTSC, PAL or other formats, for example, in realtime at least 10 to several dozen times within 1/30 to 1/60 second.

Please delete the text at page 18, lines 4 – 6.

Please replace the paragraph beginning at page 26, line 4 with the following:

BO

The above processing is repeatedly executed until the variable n is not judged to be less than 2 (that is, until $n=2$) in step S81. The processing described above causes the results of multiplying by each of the elements of the 3×3 array of convolution filter coefficients to be repeatedly rendered and added to the same destination pixel data $C_{dp}[i][j]$. That is, the convolution filtering of a single subject pixel is completed.

Please delete the text at page 28, line 4.